

Parallel Processing Lab

FPGA & Embedded Systems Lab

COLLEGE: GOA COLLEGE OF ENGINEERING

RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2019

Course: Revised Course - 2013

Seat No: 3201 PRI	No: 201309124	Sex: M	Nam	e: DHURI VIBHAV LAXMANNATH	
No Of Attempts: 1		No Of Credits	Grad Obtai	0004	
ASIC Design & FPGA					
	Theor	у 4	BB	P	
	IA	2	AB	P	
Digital Signal Process	ors & Embedded Systems				
	Theor	y 4	ВВ	P	
	IA	2	ВС	P	
Design for Testability	& E-Waste Management				
	Theor	y 4	ВВ	P	
	IA	2 .	AA	P	
Processor Architecture	e & Parallel Processing				
93	Theor	y 4	ВВ	P	
	IA	2	BB	P	
Memory Design					
, , ,	Theor	y 4	ВВ	P	
	IA	2	ВС	Ρ .	

2

2

2

2

38

ВВ

BB

AB P

BB P

7.11 P PASSES

IA

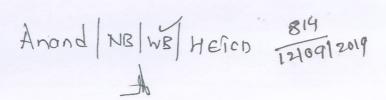
IA

Practical

Practical

Total:

Seat No: 3202	P R No : 201401159	Se	x : M	Nan	ne :	KSHIRSAGAR MADHAV ALIAS PRASAD	CHARLES (MAIL)
No Of Attempts: 1			No Of Credits	Gra Obta		SGPA	
ASIC Design	& FPGA						
		Theory	4	ВС	P		
		IA	2	AB	Р		
Digital Signa	Processors & Embedded S	ystems					
		Theory	4	BB	P		
		IA	2	CC	P		
Design for Te	estability & E-Waste Manage	ement					
		Theory	4	BB	P		
		IA	2	AO	P		
Processor Ar	chitecture & Parallel Process	sing					
		Theory	4	AB	P		
		IA	2	AB	P		
Memory Des	gn						
		Theory	4	CC	P	1	
		IA	2	AB	P		
Parallel Proc	essing Lab						
		IA	2	AB	P		
		Practical	2	AB	P		
FPGA & Emb	edded Systems Lab						
		IA	2	AB	P		
		Practical	2	AA	P		
		Total:	38	***************************************	*************	7.26 P	









RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2019 Course: Revised Course - 2013

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COLLEGE.	GUA	CULLEGE	UL	ENGINEERING

Seat No: 3203 PR No: 201408325	Se Se	x: F	Nam	ne: LO	BO JOELLA	
No Of Attempts: 1		No Of Credits	Gra		SGPA	
ASIC Design & FPGA						
	Theory	4	BB	P		
	IA	2	AA	P		
Digital Signal Processors & Embedded	Systems					
	Theory	4	BB	P		
	IA	2	AA	P		
Design for Testability & E-Waste Mana	gement					
	Theory	4	BB	P		
	IA	2	AA	P		
Processor Architecture & Parallel Proc	essing					
	Theory	4	AB	P		
	IA	2	AB	P		
Memory Design						
	Theory	4	AB	P		
	IA	2	AA	P		
Parallel Processing Lab						
	IA	2	AB	P		
	Practical	2	AB	P		
FPGA & Embedded Systems Lab						
	IA	2	AB	P		
	Practical	2	AB	P		
	Total:	38	waaana na waa co waa aa	www.come.com/20040404000000000000000000000000000000	7.89 P PASSES	#21000000000000000000000000000000000000

Seat No: 3204 PR No: 201406699	Se	x: F	Nam	ne: I	NAIK AKSHATA UDAY
No Of Attempts: 1		No Of Credits	Grad Obtai		SGPA
ASIC Design & FPGA					
	Theory	4	AA	P	
	IA	2	AA	P	
Digital Signal Processors & Embedded S	Systems				
	Theory	4	AB	P	
	IA	2	AA	P	
Design for Testability & E-Waste Manag	ement				
	Theory	4	BB	P	
	IA	2	BB	P	
Processor Architecture & Parallel Proces	ssing				
	Theory	4	AA	P	
	IA	2	AA	P	
Memory Design					
	Theory	4	BB	P	
	IA	2	AA	P	
Parallel Processing Lab					
	I.A	2	AB	P	
	Practical	2	AB	P	
FPGA & Embedded Systems Lab					
•	IA	2	BC	P	
	Practical	2	ВС	P	
	Total:	38	***************************************	***************	7.95 P PASSES



RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2019 Course: Revised Course - 2013

COLLEGE: GOA COLLEGE OF ENGINEERING

FPGA & Embedded Systems Lab	IA	2	AA	Р	
EDOA A Fash added Contains Lab	Practical	2	AA	Р	
	IA	2	AB		
Parallel Processing Lab					
	IA	2	A.A	P	
	Theory	4	BC	P	
Memory Design					
	IA	2	AA	Р	
93	Theory	4	ВВ	Р	
Processor Architecture & Parallel Proces	ssing				
	IA	2	AB	P	
Design for restability & E-vvaste Manag	Theory	4	CC	Р	
Design for Testability & E-Waste Manag		2	ЪС		
	IA	2	BC	Р	
Digital Signal Processors & Embedded	Theory	4	ВВ	Р	
District Circust Drassesson 9 Embodded	IA	2	AA	P	
	Theory	4	BC	P P	
ASIC Design & FPGA			-	-	
o Of Attempts: 1		No Of Credits	Gra Obta		SGPA
eat No: 3205 P R No: 201308747	36	x: M			NGSE PRANAV MANJANATH

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
ВВ	7	Good
ВС	6	Fair
СС	5	Satisfactory
FF	0	Fail

Checked By :

Date:

Aniketh Gaonkar Assistant Registrar-E(Proff.)

Prof. Anuradha Wagle Controller Of Examinations

Prof. Y. V. Reddy Registrar

